Andrew Fowler

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Permanent Address
9722 Sugar Hill Dr
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Education

University of Florida located in Gainesville, FL.

- **Major: Computer Engineering (Hardware) awarded 2013**

Notable Skills

UVM, SystemVerilog – Used while writing testbench code
Computer Architecture – Validation on out of order A-class ARM cores used in premium mobile, clamshell laptops and servers.
Scripting Languages- Python for instruction generation from XML and **Ruby** for log parsing and RTL generation from Excel spreadsheets**.**
Atlassian products such as **Bamboo** for continuous integration of smokes and **Jira** for bug reporting**.**

Work Experience

Design Engineer, ARM; Austin, TX; June 2015 - Present

- Front end validation for a superscaler out of order processor on the Decode, Rename, Issue, and Commit units all written in system verilog in a UVM test bench environment using mostly random testing and assertion testing.
- Recreate customer fails with directed tests and work with them to create a software solution.
- Wrote models for units that interact with the core including loadstore and fetch along with all drivers and checkers for each boundary.
- Scripts written in python and perl including instruction generation, coverage generation, and architecture rule checking.

Graduate Design Engineer- 3 rotations, ARM; Austin, TX; Jan 2014 - June 2015

- Validation for Level 2 cache which mostly involved coherency checking and interaction with the interconnect.
- Performance testing for an enterprise DDR Memory controller. Deep dive into where latency was coming from and how to reduce it.
- Implementation for the full CPU layout on Cortex-A57 mostly working with tools and TCL scripting.

Design Engineer Intern, ARM; Austin, TX; Summer 2013

- Worked on the validation team for the loadstore unit in the new Corex A57 ARM core that will go in higher power envelope devices such as tablets.
- Used Data preloading so we could have more useful cycles sooner in the test. Adding nonzero data, changing line states, etc all allowed for higher quality checks while the testbench would have been waiting for cache fills.

Product Development Co-op Engineer, AMD; Austin, TX; Fall 2011 and Fall 2012

- High Speed I/O Advanced Testing and Characterization team
- All analog PHY testing with PCIe, DisplayPort, and USB phys.
- Worked with Verigy and Credence Automated Test Equipment
- Automated data processing using Perl and Genesis.
- Gained teamwork skills while working on collaborative projects.
- Test Time reduction efforts for production tests

Check out my website for more info: http://plaza.ufl.edu/andarooo/